

AMENDMENTS TO THE CLAIMS

Claims 1-16 (cancelled).

Mute!

17. (Currently Amended) A transistor formed on a substrate assembly, comprising:

- a raised drain structure;
- a raised source structure;
- a gate located between said source and said drain;
- a first capping layer in communication with at least a portion of said gate and said source;
- a first portion of a gate oxide region in communication with at least a portion of said gate and said source;
- ~~said source, said gate, said first capping layer, and said first portion of said gate oxide region defining a first gap therein, said first gap having one of a gas and a vacuum therein, wherein no dielectric material is positioned between said first gap and any one of said gate, said source, said first capping layer, and said first portion of said gate oxide region;~~
- a first implant junction area located in said substrate assembly beneath said first gap and extending partially beneath said gate and said source;
- a second capping layer in communication with at least a portion of said gate and said drain;
- a second portion of said gate oxide region in communication with at least a portion of said gate and said drain; and
- ~~said drain, said gate, said second capping layer, and said second portion of said gate oxide region defining a second gap therein, said second gap having one of a gas and~~

~~a vacuum therein, wherein no dielectric material is positioned between said second gap and any one of said gate, said drain, said second capping layer, and said second portion of said gate oxide region; and~~

~~a second implant junction area located in said substrate assembly beneath said second gap and extending partially beneath said gate and said drain.~~

Claim 18 (cancelled).

D1 number > 19. (Original) The transistor of claim 17 wherein said first and second junctions include doped areas.

Claims 20-97 (cancelled).

sub E1 > 98. (Previously Added) The transistor of claim 17, wherein said raised source includes doped polysilicon.

99. (Previously Added) The transistor of claim 17, wherein said raised drain includes doped polysilicon.

100. (Previously Added) The transistor of claim 17, wherein said gate includes doped polysilicon.

101. (Previously Added) The transistor of claim 17, wherein said source includes a plug.

102. (Previously Added) The transistor of claim 101, wherein said plug includes an adhesive layer.

103. (Previously Added) The transistor of claim 17, wherein said gate includes a gate terminal.

Claims 104-124 (cancelled).

Mixed > 125. (Currently Amended) A transistor formed on a substrate assembly, comprising:

a raised drain structure;

a raised source structure;

a gate located between said source and said drain;

a first capping layer in communication with at least a portion of said gate and said source;

a first portion of a gate oxide region in communication with at least a portion of said gate and said source;

~~said source, said gate, said first capping layer, and said first portion of said gate oxide region defining a first gap therein, said first gap having one of a gas and a vacuum therein, wherein no dielectric material is positioned between said first gap and any one of said gate, said source, said first capping layer, and said first portion of said gate oxide region;~~

a first implant junction area located in said substrate assembly beneath said first gap and extending partially beneath said gate and said source, wherein said first junction area includes doped silicon areas;

a second capping layer in communication with at least a portion of said gate and said drain;

a second portion of said gate oxide region in communication with at least a portion of said gate and said drain; and

~~said drain, said gate, said second capping layer, and said second portion of said gate oxide region defining a second gap therein, said second gap having one of a gas and a vacuum therein, wherein no dielectric material is positioned between said second gap~~

~~and any one of said gate, said drain, said second capping layer, and said second portion of
said gate oxide region; and~~

~~a second implant junction area located in said substrate assembly beneath said
second gap and extending partially beneath said gate and said drain, wherein said second
junction area includes doped silicon areas.~~

126. (Previously Added) The transistor of claim 125, wherein said doped silicon
areas include phosphorous.

Claim 127 (cancelled).

128. (Currently Amended) A transistor formed on a substrate assembly, comprising:
~~ube!~~
a raised drain structure;
a raised source structure;
a gate located between said source and said drain;
a first capping layer in communication with at least a portion of said gate and said
source;
a first portion of a gate oxide region in communication with at least a portion of
said gate and said source;
~~said source, said gate, said first capping layer, and said first portion of said gate
oxide region defining a first gap therein, said first gap having one of a gas and a vacuum
therein, wherein no dielectric material is positioned between said first gap and any one of
said gate, said source, said first capping layer, and said first portion of said gate oxide
region;~~

a first implant junction area located in said substrate assembly ~~beneath said first gap and~~ extending partially beneath said gate and said source, wherein said first junction area includes a pocket implant junction;

a second capping layer in communication with at least a portion of said gate and said drain;

a second portion of said gate oxide region in communication with at least a portion of said gate and said drain; and

~~said drain, said gate, said second capping layer, and said second portion of said gate oxide region defining a second gap therein, said second gap having one of a gas and a vacuum therein, wherein no dielectric material is positioned between said second gap and any one of said gate, said drain, said second capping layer, and said second portion of said gate oxide region; and~~

a second implant junction area located in said substrate assembly ~~beneath said second gap and~~ extending partially beneath said gate and said drain, wherein said second junction area includes a pocket implant junction.
